

**Amendments to the Claims**

This listing of claims will replace all prior versions and listings of claims in the application:

**Listing of claims:**

1. (canceled)
2. (Currently Amended) The method of claim 7 wherein the first control bit is set by a programmer.
3. Currently Amended) The method of claim 7 further comprising:  
handling the output signal as an STS connection when the first control bit is set.
4. (Currently Amended) The method of claim 7 further comprising:  
assembling the output signal from multiple VT/TU connections when the first control bit is not set.
5. (Currently Amended) The method of claim 7 further comprising:  
handling the output signal as the AU connection when the first control bit is not set.
6. (Currently Amended) The method of claim 7 further comprising:  
assembling the output signal from multiple VT connections when the first control bit is set.
7. (Currently Amended) A method of processing an output signal comprising:  
checking a state of a first control bit that specifies whether to assemble the output signal from multiple virtual tributary connections or handle the output signal as an synchronous transport signal (STS) or administrative unit (AU) connection;  
switching a predetermined number of connection entries together based on the state of the first control bit;  
storing the first control bit in a connection memory;

checking a state of a second control bit that is associated with independent and concatenated payloads; and

cross-connecting a second payload with a first payload if the second control bit is set.

8. (Currently Amended) The method of claim 7 further comprising storing the first control bit in a register.

9. (canceled)

10. (canceled)

11. (canceled)

12. (Previously Presented) The method of claim 7 further comprising:  
processing a second payload independently of a first payload if the second control bit is not set.

13. (Currently Amended) The method of claim 7 further comprising storing the second control bit in athe connection memory.

14. (previously presented) The method of claim 7 further comprising storing the second control bit in a register.

15. (canceled)

16. (canceled)

17. (Currently Amended) The core logic of claim 18 wherein the first control bit is set by a programmer.

18. (Currently Amended) A core logic and memory for provisioning cross-connects in an output signal in network switching environment comprising instructions for causing a computer said core logic to:

check a state of a first control bit that specifies whether to assemble the output signal from multiple virtual tributary/tributary unit (VT/TU) connections or handle the output signal as an synchronous transport signal (8T8) or administrative unit (AU) connection;

switch a predetermined number of connection entries together based on the state of the first control bit;

store the first control bit in a connection memory;

check a state of a second control bit that is associated with independent and concatenated payloads; and

cross-connecting a second payload with a first payload if the second control bit is set.

19. (Currently Amended) The core logic of claim 18 further comprising instructions to store the first control bit in a register.

20. (canceled)

21. (Currently Amended) The core logic of claim 18 further comprising instructions to store the second control bit in a-the connection memory.

22. (Previously Presented) The core logic of claim 18 further comprising instructions to store the second control bit in a register.

23. (canceled)

24. (Currently Amended) Apparatus for processing an output signal comprising:  
a first memory storing a first control bit that specifies whether to assemble the output signal from multiple virtual tributary (VT) connections or handle the output signal as an synchronous transport signal (8T8) or administrative unit (AU) connection;  
a circuit to check a state of the first control bit; and  
control circuitry that uses a second memory to switch a predetermined number of connection entries together based on the state of the first control bit;

a memory storing a second control bit that is associated with independent and concatenated payloads; and

a circuit to cross-connect a second payload with a first payload if the second control bit is set.

25. (Currently Amended) The apparatus of claim 24 wherein the control circuitry is configured to handle the output signal as an STS connection when the first control bit is set.
26. (Currently Amended) The apparatus of claim 25 wherein the control circuitry is configured to assemble the output signal from multiple VT connections when the first control bit is not set.
27. (Previously Presented) The apparatus of claim 24 wherein the control circuit is configured to switch a predetermined number of payloads together based on the state of the second control bit.